CLAIMS

What is claimed is:

1. A switching matrix comprising:

a field programmable gate array having an input memory and an output memory; and

wherein the field programmable gate array stores in the input memory an input frame having a plurality of input channels; and

wherein the field programmable gate array stores in the output memory an output frame having a plurality of output channels is stored;

wherein the field programmable gate array further includes a map memory in which the field programmable gate array stores at least one mapping that specifies one of the plurality of input channels that is mapped to one of the output channels.

2. The switching matrix of claim 1, wherein each of the input channels corresponds to one of a plurality of time slots.

3. The switching matrix of claim 1, wherein each of the output channels corresponds to one of a plurality of time slots.

4. The switching matrix of claim 1, wherein the input memory includes a plurality of banks of memory in which a plurality of input frames are stored by the field programmable gate array.

5. The switching matrix of claim 1, wherein the input memory includes a plurality of banks of memory in which a

plurality of input frames are stored by the field programmable gate array.

6. The switching matrix of claim 1, wherein the field programmable gate array includes a logic block that includes an input interface, wherein the input interface stores the input frame in the input memory.

7. The switching matrix of claim 1, wherein the field programmable gate array includes a state machine block, wherein the state machine block reads one of the plurality of input channels of the input frame stored in the input memory and writes the input channel to one of the plurality output channels of the output frame stored in the output memory.

8. The switching matrix of claim 7, wherein the state machine block reads the mapping from the map memory.

9. The switching matrix of claim 1, wherein the input memory includes a dual ported random access memory.

10. The switching matrix of claim 1, wherein the output memory includes a dual ported random access memory.

11. A switching matrix comprising:

means for storing an input frame having a plurality of input channels;

means for storing an output frame having a plurality of output channels; and

means for mapping at least one of the input channels of the input frame to a corresponding one of the plurality of output channels of the output frame.

12. The switching matrix of claim 11, wherein the means for mapping includes:

means for reading the at least one of the input channels of the input frame from the means for storing the input frame; and

means for writing to the means for storing the output frame the at least one of the input channels of the input frame in the corresponding one of the plurality of channels of the output frame.

13. A switching matrix comprising:

an input memory;

an output memory; and

a field programmable gate array that stores in the input memory an input frame having a plurality of input channels and that stores in the output memory an output frame having a plurality of output channels; and

wherein the field programmable gate array includes a map memory in which the field programmable gate array stores at least one mapping that specifies one of the plurality of input channels that is mapped to one of the output channels.

14. The switching matrix of claim 13, wherein the input memory is included in the field programmable gate array.

15. The switching matrix of claim 13, wherein the output memory is included in the field programmable gate array.

16. The switching matrix of claim 13, wherein the field programmable gate array receives each of the plurality of input channels from an input source and stores each of the plurality input channels in the input memory.

17. The switching matrix of claim 16, wherein the field programmable gate array reads one of the plurality of input channels stored in the input memory and writes the input channel to one of the plurality output channels of the output frame stored in the output memory.

18. The switching matrix of claim 13, wherein each of the input channels corresponds to one of a plurality of time slots and each of the output channels corresponds to one of a plurality of time slots.

19. The switching matrix of claim 13, wherein the input memory includes a plurality of banks of memory in which a plurality of input frames are stored by the field programmable gate array and the input memory includes a plurality of banks of memory in which a plurality of input frames are stored by the field programmable gate array.

20. The switching matrix of claim 13, wherein the input memory includes a dual ported random access memory and the output memory includes a dual ported random access memory.